An Audio Boost Circuit

This patent application is a continuation-in-part application of parent application having serial number 09/439,119 filed 11/12/99.for an Audio Boost Circuit having a common inventor and assignee.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to the field of electronics amplifiers and more particularly to the field of signal conditioning circuits for signal boosting in within a predetermined bandwidth so as to compensate for reduced speaker performance resulting from reduced woofer size.

2. Description of Related Art:

U.S. Patent 5,736,897 for a Low Input Signal Bandwidth Compressor & Amplifier Control Circuit with a State-variable Pre-Amplifier issued on April 7, 1998 to Paul Gagon who assigned the invention to BBE Sound of Huntington Beach, California. The contents of U.S. Patent 5,736,897 are incorporated by reference herein in its entirety. The inventor and assignee are common with those for the present invention. The `897' patent shows the use of a state-variable filter. The `897' reference does not show or teach the use of an Infinite Gain Multiple Feedback Band-Pass Filter in combination with a State-Variable Band-Pass Filter acting as a pre-amplifier.

SUMMARY OF INVENTION

In a first embodiment, the invention audio boost circuit has input buffer responsive to a program input signal having high, low and mid-range frequency signal components for providing a buffered program signal. The buffered program signal is fed to an all pass phase inverter having an input coupled to receive the buffered program signal and an output providing an inverted buffered program signal, The buffered program signal is also fed to a band pass filter having a predetermined Q, responsive to the buffered program signal for providing an inverted band pass boosted program signal. A summing amplifier adds the inverted buffered program signal to the inverted band pass boosted program signal to provide a composite program signal signal as an output signal to a power amplifier and speaker combination. In a more particular embodiment, the band pass filter has a peak gain at a center frequency, and, a frequency adjustment means is provided for adjusting the frequency at which the peak gain occurs. In a yet more particular embodiment, the band pass filter has a first second and third resistor and a first and second capacitor, and the band pass filter's first, second and third resistor values and the values of the first and second capacitors are selected to obtain a Q in the range of from 3 to 6, and a frequency adjustment resistor in series with the second resistor is adjusted to position the peak gain at a frequency in the range of 50 to 100 cycles/sec.

A second alternative embodiment of the invention audio boost circuit comprises an input buffer responsive to a program input signal having high, low and mid-range frequency signal components for providing a buffered program signal, the

input buffer comprises: a state-variable filter for processing the input program signal into high, low and mid-range frequency compensated signal components. The state-variable filter comprises: a first amplifier stage responsive to the program signal that provides a high frequency compensated signal; a second amplifier stage responsive to an output of the first amplifier stage that provides a mid-range compensated signal; and, a third amplifier stage responsive to an output of the second amplifier stage that provides a low range compensated signal.

The input buffer further comprises: a state-variable summing amplifier for adding the high frequency compensated signal, the low frequency compensated signal and the mid-range compensated signal and an adjusting means for adjusting the gain between the high frequency compensated signal and the mid-range compensated signal; and the low frequency compensated signal to provide the buffered program signal.

The input buffer is followed by an all pass phase inverter having an input coupled to receive the buffered program signal and an output that provides an inverted buffered program signal, A band pass filter with a predetermined Q, is coupled to the buffered program signal to provide an inverted band pass boosted program signal, A summing amplifier adds the inverted buffered program signal to the inverted band pass boosted program signal to provide a composite program signal. A power amplifier and speaker respond to the composite program signal to producing an audible sound in response to the composite program signal.

In a more particular second embodiment, of the state-

variable filter, the mid-range signal components are inverted in phase with respect to the high and low frequency signal components and the state-variable filter further comprises: a first amplifier stage having an inverting and non-inverting input. The program signal is coupled to the inverting input; and a resistor divider network is coupled to the mid-range compensated signal. The resistor divider network has an output that provides a portion of the mid-range compensated signal to the first amplifier non-inverting input.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1. is a block diagram of the audio boost circuit;

Figure 2 is a schematic of the block diagram of Figure 1 showing a first embodiment of an input buffer, the all pass phase inverter, the constant Q band pass filter and the summing amplifier.

Figure 3 is an expanded block diagram of Figure 1 showing a second embodiment of the input buffer;

Figure 4 is a schematic of the expanded block diagram of the second embodiment of the input buffer.

PREFERRED EMBODIMENT

Figure 1. is a block diagram of the audio boost circuit 10 showing an input buffer 12 having an input 14 and an output at terminal 16. An all pass phase inverter 18 has its input connected to terminal 16 and its output is connected to terminal 20. A constant Q band pass filter 22 has its input connected to terminal 16 and its output connected to terminal 24. Summing amplifier 26 has a first input connected to terminal 20, a second input connected to terminal 24 and an output connected to terminal 28. Block 30 represents a power amplifier having an input connected to the transfer contact 32 of switch 34. The power amplifier output 36 is shown connected to a speaker 38.

The input buffer 12 is coupled to receive a program input signal at input terminal 14. The program input signal is typically received from a tape player or a CD reader. Such signals typically contain audio information such as recorded music and have amplitudes in the range of 150 mV RMS and have high, low and mid-range frequency audio signal components for providing a buffered program signal at terminal 16.

The all pass phase inverter 18 has an input coupled to receive the buffered program signal at terminal 16 and an output providing an inverted buffered program signal to terminal 20.

The band pass filter 22 is designed to have a predetermined Q with a center frequency that is empirically selected to optimize the performance of the power amplifier 30 and speaker 38. The band pass filter 22 is connected to receive

the buffered program signal from terminal 16 and amplify and phase invert a narrow range of low frequency of the buffered program signal to provide an inverted band pass boosted program signal to terminal 24,

Summing amplifier 26 adds the inverted buffered program signal received at its first input from terminal 20 to the inverted band pass boosted program signal received at its second input from terminal 24 and outputs the sum of the signals as a composite program signal signal at terminal 28.

Figure 2 is a schematic of a first embodiment of the audio boost circuit. The component values show were used in a circuit that was built and tested. Phantom block 12 shows the input buffer comprising a simple unity gain non-inverting amplifier. An inverting unity gain amplifier would work equally as well. The amplifier shown in 1/4 of a TL072. The 10 uF capacitor is a dc blocking capacitor. The 100 pF capacitor is for high frequency noise suppression. A second embodiment of the input buffer using a state-variable filter is discussed later in connection with Figures 3 and 4.

The all pass phase inverter within phantom block 18 is an inverting unity gain amplifier. The 100 pF capacitor is used to enhance the stability of the operational amplifier. The band pass filter within phantom block 22 is designed to have a predetermined Q in the range of from 3 to six. The Q selected and the center frequency selected are empirically determined with the power amplifier and speaker combination for best results. The band pass filter has resistors first second and third resistors 40, 42 and 44 respectively, each resistor having a first and second terminal, The filter also

has a first and second capacitor, 46 and 48 respectively each capacitor having a first and second terminal. Operational amplifier 50 has an inverting input, a non-inverting input and an output connected to terminal 24.

The first resistor 40 first terminal is coupled to terminal 16 to receive the buffered program signal. The first resistor second terminal is coupled or connected to node 52. The second resistor 42 first terminal and the first terminal of the first and second capacitors 46, 48 are also connected to node 52.

The second resistor 42 second terminal is connected to a reference potential such as ground. In the embodiment of Figure 2, adjustable resistor 54 is connected in parallel with resistor 56 and the pair are in series with resistor 42 to form a frequency adjustment means for adjusting the frequency at which the peak gain of the band pass filter 22 occurs. The adjustment means could be a single equivalent value resistor selected to replace the second resistor 42 in series with the parallel combination of the adjustable resistor 54 and resistor 56.

The first capacitor 46 second terminal is connected to the operational amplifier's inverting input and to the third resistor's 44 first terminal. The second capacitor's 48 second terminal is connected to the operational amplifier's output terminal and to the third resistor's 44 second terminal.

The band pass filter of phantom block 22 is referred to as an infinite gain multiple feedback band pass filter. The design of an infinite gain multiple feedback band pass

filter such as shown in phantom block 22 in Figure 2 is taught with examples given in the text "The Active Filter Handbook" by Frank P. Tedeschi, pg 160 - 168, Tab Books Inc of Blue Ridge Summit, Pa., 17214.

An alternative discussion with design examples is found in the "Handbook Of Operational Amplifiers Active RC Networks" 1966, at pages 32 - 34 and 78 - 79, published by the BURR-BROWN RESEARCH, CORPORATION, INTERNATIONAL AIRPORT INDUSTRIAL PARK, TUCSON, ARIZONA 85706.

However, the topology for a set of design requirements is not unique nor are the values for a given topology. The following example and equations show how the component values are determined for an circuit in which the Q, center frequency f and the peak gain Ao are given. In general, the Q of a band-pass filter is defined as the bandwidth divided by the center frequency. Assume that the center frequency required is 78.8 Hz. Assume that the Q required is 5.4 and the peak gain Ao required is 1.03. The first and second capacitors have the same value which is defined as c. A convenient value of 0.39 uF is selected for a first try. Using the design procedure found in the "Handbook Of Operational Amplifiers Active RC Networks" mentioned above:

$c \equiv 0.39 \cdot 10^{-6}$ $Q \equiv 5.4$ $f \equiv 78.7$ $Ao \equiv 1.03$

$a := \frac{1}{Q}$ $k \equiv 2 \cdot \pi \cdot f \cdot c$ $\pi \equiv 3.14159$

$a = 0.185$ $k = 1.928 \cdot 10^{-4}$ $H := \frac{Ao}{Q}$

$$R1 := \frac{1}{H \cdot k} \qquad R2 := \frac{1}{(2 \cdot Q - H) \cdot k} \qquad R3 := 2 \cdot \frac{Q}{k}$$

$$R1 = 2.719 \cdot 10^4 \qquad R2 = 488.76 \qquad R3 = 5.6 \cdot 10^4$$

With a Q of 3 specified, the following values of resistors were calculated using the same value of capacitors:

$$R1 = 1.51 \cdot 10^4 \qquad R2 = 916.686 \qquad R3 = 3.111 \cdot 10^4$$

The values of R1, R2 and R3 corresponds to the values of the first, second and third resistors in the previous example. It can be seen that the values of resistors are obtainable for the range of Q of 3 to 6 that is desired. The frequency adjustment resistor 54 and the values of resistors 42 and 56 which combine to form R2 in the calculations above are calculated or determined empirically to position the peak gain at a frequency in the range of 50 to 100 herts.

The summing amplifier within phantom block 26 represents a means for adding the inverted buffered program signal to the inverted band pass boosted program signal and for providing a composite program signal. Resistor 58 has a first and second terminal. The first terminal of resistor 58 is connected to terminal 20 to receive the inverted buffered program signal. The second terminal of resistor 58 is connected to the inverting input of operational amplifier

and to the first terminal of the feed-back resistor 62. The second terminal of the feedback resistor 62 is connected to the output of the summing amplifier terminal 28.

Resistor 64 and 66 in series have a first and second terminal. The first terminal of the series combination is connected to terminal 24 to receive the inverted buffered program signal. The second terminal of the series combination is also connected to the inverting input of operational amplifier and to the first terminal of the feed-back resistor 62. The first terminal of the series combination is connected terminal 24 to receive the inverted band pass boosted program signal from the band pass filter.

Adjustable resistor 66 in series with resistor 64 represent a boost adjusting resistor in series with the second input to the summing amplifier for adjusting the relative gain of the inverted buffered program signal with respect to the inverted band pass boosted program signal.

Figure 3 is shows the block diagram of a second alternative embodiment of the input buffer 12 using a state-variable filter 72 responsive to the program input signal at terminal 14 having high, low and mid-range frequency signal components. This second embodiment of the input buffer 12 has a state-variable filter 72 and a state-variable summing amplifier 74 for adding the high, low and mid-range frequency signal components to provide the buffered program signal.

The state-variable filter has a first amplifier stage 90

responsive to the program signal for providing a high frequency compensated signal; a second amplifier stage 98 responsive to an output of the first amplifier stage for providing a mid-range compensated signal; and a third amplifier stage 104 responsive to the mid range compensated signal for providing a low range compensated signal.

In Figure 4, the input buffer 12 has gain control circuitry within the state-variable summing amplifier 74, such as adjustable resistors 114 and 116, for balancing and summing the high and mid-range signals.
The state-variable filter within phantom box 72 is coupled or connected to the program input signal at terminal 14 and processes the program input signal into high, low and mid-range frequency signal components. The state-variable summing circuit 74 adds the high frequency compensated signal, the low frequency compensated signal and the mid-range compensated signal to provide the buffered program signal at terminal 16. The input buffer also provides an adjusting means within the state-variable summing amplifier 74 for adjusting the gain between the high frequency compensated signal and the mid-range signal.

The three band-pass signals comprise a low band-pass signal Vlp (a low-range compensated signal) on signal line 76, a mid-range bandpass signal Vmp (a mid-range compensated signal) on signal line 78 and a high range bandpass signal, Vhp (a high frequency compensated signal) on signal line 80 to respective inputs of a state-variable summing amplifier 74. The mid-range signal components produced by the state-variable filter 72 are inverted in phase with respect to the phase of the high and low frequency signal components produced by the state-variable filter 72.

Figure 4 shows that the state-variable summing amplifier 74 uses operational amplifier 82 and sums the respective Vlp, Vmp and Vhp signals at the low pass input 84, the mid-range input 86 and the high pass input 88, and provides the buffered program signal at output terminal 16 to the all pass phase inverter 18 and to the band pass filter 22 as shown in Figure 1 ,or via switch 34, directly to power amplifier 30 to drive speaker 38.

As explained in U.S. Patent 5,736,897 for a Low Input Signal Bandwidth Compressor & Amplifier Control Circuit with a State-variable Pre-Amplifier issued on April 7, 1998, the combination of the state-variable filter 72 and the state-variable summing amplifier 74 form a functional and lower cost equivalent of the alternative embodiment three channel pre-amplifier shown in Figures 1 and 2 in the `897' patent.

Referring again to Figures 3 and 4, phantom block 90 represents an input summing and damping amplifier circuit. The program input signal at terminal 12 and the low bandpass signal Vlp on signal line 76 are fed to the inverting input of amplifier 92. A portion of the mid-range band-pass signal Vmp is fed to the non-inverting input of amplifier 92 for damping via the damping input 94. The resulting output of amplifier 92 was the high frequency signal component Vhp at amplifier output 96 which was connected to signal line 80,

The high range band-pass signal Vhp is then connected to the negative input of a first integrator shown within phantom block 98, for inversion and integration and to the state-variable summing amplifier 74 high pass input 100 on signal line 80.

The first integrator 98 integrates the Vhp signal to provide the mid-range band-pass signal Vmp at first integrator output 102. The mid-range bandpass signal Vmp is fed to the damping input 94 of the input summing and damping amplifier circuit 90 and to the state-variable summing amplifier 92 mid-range band-pass input 86 on signal line 78.

Phantom block 104 represents a second integrator that responds to the mid-range bandpass signal Vmp on signal line 78 and provides a low bandpass signal Vlp at the second integrator output terminal 106 to the state-variable summing amplifier 74 low band-pass signal input 84 via signal line 76. The low bandpass signal Vlp is also fed to a second input 108 of the input summing and damping amplifier circuit 90.

The damping circuit of the input summing and damping amplifier circuit 90 comprises an input resistor 110 that has a first terminal connected to receive the mid-range bandpass signal at damping input 94. The second terminal of resistor 110 is coupled to the first terminal of resistor 112 and to the non-inverting input of operational amplifier 92. The second terminal of resistor 112 is coupled to a reference potential such as ground. The ratio of resistors 110 and 112 establish the "Q" of the state-variable filter. The higher the gain, of the ratio of the resistors 110 and 112, the higher the Q. The Q of the state-variable filter of Figures 3 and 4 is typically in the range of 0.5 to 2 for audio applications. The Q of the circuit of Figure 4 is approximately 0.67.

One of the objectives of the state-variable filter 72 is to set phase shift and gains up such that the mid-range band-

pass frequency signals are about 180 degrees out of phase with the signal components in the lower frequency band and in the higher frequency band. The ratio of the damping resistors, the gains and break frequencies of the amplifiers and integrator are set for a desired Q and bandpass.

The state variable summing amplifier 74 has a low frequency band-pass gain adjustment pot 114, and a high range band-pass frequency gain adjustment pot 116 that permit the user to make a final adjustment for a particular circuit and component configuration. The adjustable inputs to the state variable summing amplifier 74 permit the user to obtain additional gain for the Vhp and Vlp signal.

The state variable input buffer circuit of Figures 3 and 4 can be adjusted to obtain a total of 360 degrees of phase shift of the high frequency signal components of the input program signal with respect to the low frequency signal components of the input program signal, in frequency space over the range of 0 - 20,000 Hz. The high frequency components gain 360 degrees with respect to the lows.

The state variable pre-amplifier also provides a time delay that is adjusted to obtain about 2.5 ms time delay at 20 Hz. The 20 Hz components are physically delayed in real time by up to 2.5 ms with respect to the High Frequency components. The design objectives for audio applications are taught in U.S. Patent 4,638,258 issued on January 20, 1987 for a Reference Load Amplifier Correction System, to Robert C. Crooks. The contents of U.S. Patent 4,638,258 are incorporated herein by reference in its entirety.

Referring again to Figure 4, a reactance chart check

will show that the break frequency for the mid-range bandpass amplifier 98 to be about 2.24 KHz. The break frequency for the low range bandpass amplifier 104 is about decade lower at 224 Hz at three dB per octave. The Q of the circuit of Figure 4 is approximated by the following equation:

$$Q = (R1 + R2)/3R2 = 0.67$$

where R1 is resistor 110 and R2 is resistor 112.

Viewing the circuit heuristically, the higher reactance of the smaller cap for mid-range bandpass amplifier 98 clearly sets the gain of the amplifier to higher values at lower frequencies than that of the low range band-pass amplifier 104. It can also be seen that the mid-range band-pass amplifier is a single pole filter. The feed back signal Vmp to the damping resistors results in a controlled Q in the mid-range frequencies band.

In general, the Q of a band-pass filter is defined as the bandwidth divided by the center frequency. The design of the state variable filter of Figure 4 is taught in the text "The Active Filter Handbook" by Frank P. Tedeschi, pg 178 - 182, Tab Books Inc of Blue Ridge Summit, Pa., 17214; however, this reference does not show the outputs being summed to form the desired unbalanced output that meets the desired requirement for audio applications.

The object of the design of Figure 4 is to have a first break frequency at approximately 240 Hz and a second at 2.24 KHz, about a decade away from the first break. The low break f_c is established by the equation:

$$fc = 1/2\pi RC2$$

where R and C are the value of resistor 116 and capacitor 118. The high frequency break is set by the

$$fc = 1/2\pi RC1$$

where the value of R and $_{C1}$ are those of resistor 120 and capacitor 122.

Once the Q is selected, the ratio of R1 to R2 can be calculated from the equation. In the case of Figure 4, a Q of 0.67 was selected by knowing what the desired gain bandwidth response curve would be from the above referenced U.S. Patent 4,638,258. The circuit was modeled using a computer aided analysis program such as SPICE. The break frequencies were estimated from the information in the referenced U.S. Patent 4,638,258. Initial component values were selected based on available components. A reactance chart can be used for a quick approximation of the required remaining value once one of the values are known. The circuit shown had an initial goal of a design a center frequency at 700 Hz. At the center frequency, the gain of the circuit is about -1 dB or less than 1. The two adjustment pots, 116 and 114 permit an adjustment of the gain of the Vlp and the Vhp by about 15 dB with the values shown.

The Q was then adjusted using the pots 114 and 116 to provide the best match to the curves in the earlier patent to Crook. The Q and the break points were selected to match the response characteristic of the resulting circuit to the curves in the earlier patent to yield the same phase shifts, time delays and frequency response. The resistors 114 and

116 are set for a gain of nine but a slightly higher gain of 12 would be preferred.

The outputs Vhp, Vmp and Vlp of the state variable filer represent three independent state variables. Summing the three unbalanced outputs to obtain a buffered program signal is believed to be a novel step when combined with processing by the all pass inverter 18 in combination with the band pass filter 22 and with the resulting signals being summed by summing amplifier 26.

The procedure for adjusting the band-pass and gain as proposed in the above referenced text "The Active Filter Handbook" by Frank P. Tedeschi, at pages 178 - 182" is to set the value of C1 and C2 to be equal and to adjust the ratio of R1 and R2 and to obtain the desired Q. In the circuit of Figure 4, the state-variable summing amplifier 74 gain controls for the Vhp and Vlp signals provide for independent control of the gain and band-pass.

The above-described embodiments are furnished as illustrative of the principles of the invention, and are not intended to define the only embodiment possible in accordance with our teaching. Rather, the invention is to be considered as encompassing not only the specific embodiments shown, but also any others falling within the scope of the following claims.